Design of High-Speed FPGA based Data Acquisition System

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Abstract: The key factors which influence the overall performance of the CT system are gantry, X-ray source, high powered generator, detector and detector electronics, data transmission systems and the computer system for image reconstruction and manipulation. It is a challenge in CT Systems to enable maximum data transmission from the rotating gantry to operator console for real-time data processing. FPGA based Data Acquisition System is viable choice for gathering data with numerous channels, high precision and high sampling rate. In this study, a FPGA based Data Acquisition System for an increased data sample size has been proposed for CT Scanners. The system consists of two entities: Signal Processing Unit, Data Acquisition Unit. The Data Acquisition Unit has been designed by VHDL, simulated using Quartus II version 9.1 and implemented on Altera EP2AGX65.The main objective of the study is to enable maximum data transfer to the operator console without any losses. In the proposed Data Acquisition System, the maximum data rate was attained with a sampling frequency of 2460.

Keywords: Data Acquisition System, FPGA, VDHL, CT System.

Introduction

Industrial Systems contain contains mechanical and electrical phenomenon that are continuously changing and need to be measured. A Data Acquisition System (DAS) measures the electrical or physical phenomenon such as voltage, pressure, temperature and converts the samples into numerical values that can be manipulated by the computer.

The digital signal processing in the Data Acquisition Systems can be performed using Microcontrollers or Application Specific Integrated Circuits (ASIC) or Digital Signal Processors (DSP) or Field Programmable Gate Arrays (FPGA). The main benefits of microcontroller based DAS are its low power consumption, cost-effectiveness and compactness [3]. This system has quite a few shortcomings such as low processing speed and meager memory resources usage [2]. The reliability of microcontroller based DAS is very less. As the number of channels are increased, the efficiency of the system decreases. This is because of the serial processing nature of the processor [4]. DAS, based on ASIC's have a significant advantage in area and power. But, the fundamentally fixed nature of ASICs restricts the adaptability, and the prolonged design cycle may not justify the cost for low volume or prototype implementation. Data Acquisition System, based on DSP have features to support high performance, iterative, mathematically complex sequential tasks. However, parallelism in DSP is not very extensive. DSP is limited in performance by the clock rate and the number of useful operations it can perform per clock cycle when compared to a FPGA. Data Acquisition System using FPGA has numerous advantages namely: massive parallel data processing, long time availability, can be updated and upgraded at customer's site. Also, it is possible to have embedded soft and hard core processors onto the FPGA. This helps in design and development of low cost embedded system.

With the introduction of DSP -oriented products from Altera and Xilinx, FPGA are being considered as a solid solution for high performance signal processing applications for medical domain.

A CT (computed tomography) scan uses special X-ray equipment to take multiple images from different angles around the body. The patient is placed between the source and detector, and the detector is configured with its geometric center located at the x-ray source. Each image is an x-ray projection of a very thin transverse slice of the body. To collect the multitude of x-ray projections necessary to generate a tomographic CT image, both the x-ray source and detector are rotated about a patient within a supporting gantry. While the source and detector rotate, images are collected and stored. The three major pieces of equipment of a CT System: an imaging system that consists of a gantry and patient table, a processing system capable of processing the CT image data, and an operator's console that controls the entire imaging process and displays the final image.

Extensive studies have been carried to improve the efficiency of CT systems. Kalender *et al* (1990) introduced spiral CT Scanners which used slip-ring technology for data transmission off the rotating gantry. [7] The drawbacks of single slice CT led to development of a multi-slice CT.
Hu (1999) studied the scan and reconstruction principles of the multi-slice helical CT and the 4-slice helical CT [8]. The eight-slice CT system was introduced to enable shorter scan times, but did not yet provide improved longitudinal resolution. Hu et al. (2000) introduced CT Scanners with 16 detector rows, each of them defining 1.25-mm collimated slice width in the center of rotation [9].
Leon *et.al* (2007) have shown a method in which CT raw data can be acquired, parallel programming can be done to obtain CT images at a very low cost, improving quality, reconstruction time [1]. Murray *et al* (1998) patented for a Scalable Data Acquisition System that may be used with both single and multi-slice imaging system. [5]. Pan (2001) from patented for methods & apparatus for efficient data acquisition in CT Scanners. [6]
Flohr *et al* (2009) mentioned that the Multi-Detector row CT (MDCT) must handle high data rates with increasing the number of detector rows and decreasing the gantry rotation times. [10]
Th present CT system utilizes slip-ring to transfer data from the rotating gantry to stationary controller. Secondly, it uses Ethernet Bus to transfer data from the stationary controller to Data Storage Device at operator console. It is necessary to optimize the amount of data transferred through the above two interfaces.
As the amount of data to be transferred to the operator console increases, transmitting the data through the slip-ring becomes a bottleneck in Data Acquisition System. Also, a failure might occur while transferring data from the stationary controller to Data Storage device at the operator console. Thus, understanding the maximum data that could be transferred through the proposed data transmission system to the operator console without any loss is a necessity.
The main objectives of this study are: to configure the elements of Data Acquisition FPGA for increase in data sample size and to enable maximum data transfer to the operator console without any loss. The data rate of the system can be increased by increasing the detector rows and by increasing the sampling frequency. The sampling frequencies have been optimized for maximum utilization of the link capacity.

Data Acquisition System

The proposed Data Acquisition System used is shown in the Figure 1, which consists of a Detector Panel, Analog to Digital Converter(ADC), Data Acquisition FPGA, Stationary Controller Board, Operation Console (OC). The system can be said to consist of two modules, namely Signal Processing Unit, Data Acquisition Unit.

Signal Processing Unit:
The CT Scanner uses a clarity panel detector that has segmented panel design, delivers excellent spatial resolution to enable high quality of the image [1]. The detector has multiple modules and each module is linked to a ADC. The system contains multiple ADC ‘s which have simultaneous connections to the Data Acquisition FPGA. Each ADC provides a resolution of 16 bits. The ADC will send a continual serial data stream to the Data Acquisition FPGA.

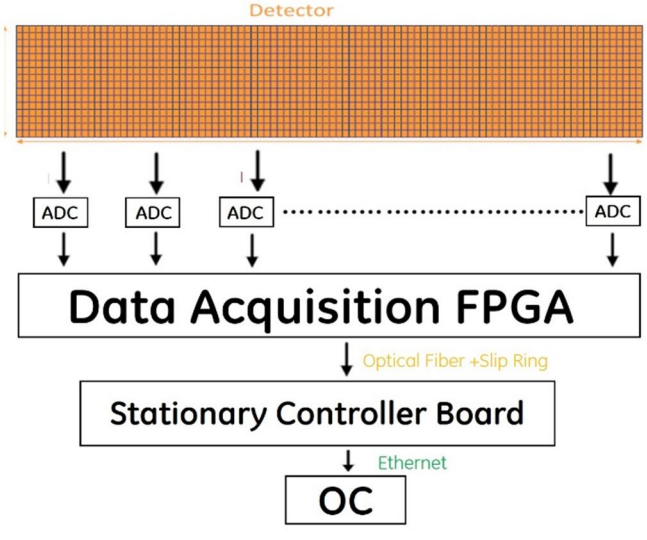

Figure 1 Proposed Data Acquisition System

Data Acquisition Unit

The main function of the Data Acquisition Unit is to collect the 16-bit data from the ADC's, restructure & process the data, transfer these data to the OC using optical interface and slip-ring technology. Quartus II version 9.1 is used for design entry using VHDL for the Altera Data Acquisition FPGA EP2AGX65.

The FPGA processes the data procured from the multiple ADC's and the format conversion begins. In Data Acquisition FPGA (Figure 2), Rx Function, FIFO and RAM Module are the configured for the increase in data sample size. RX Function is responsible for the data from the ADC to the FPGA.

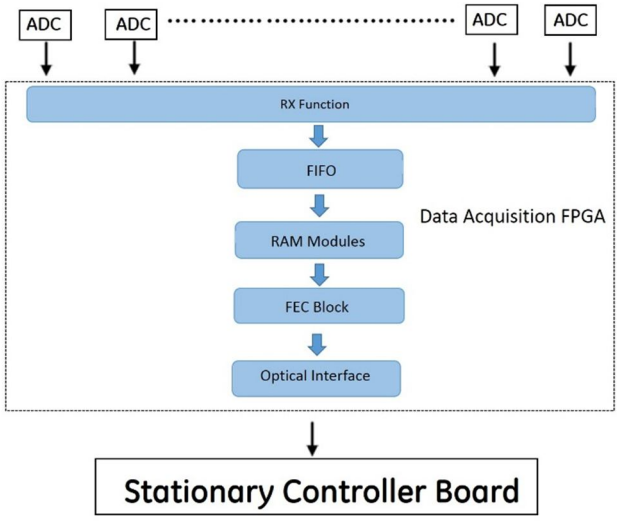

Figure 2 Modules of Data Acquisition FPGA

From the Rx Function Module, the data is written to a FIFO. Once the fifo-empty flag is enabled, the data from the FIFO is stored in the RAM Module. The ram size has been increased for increased data sample size. The final data ready for transmission is in the format shown in Figure 3.

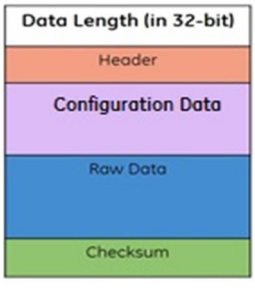

Figure 3 Final Format of Data in RAM Module

The FEC Block breaks up the final format of data obtain in RAM Module into several blocks, called message blocks, and adds a Forward Error Correction (FEC) CRC to each block immediately prior to sending to verify detect and correct errors in the message block. A serial encoding scheme of Conditional Inversion Master Transition (CIMT) is used for sending high-speed serial data, on fiber optic media. The FEC Coding scheme and the CIMT transmission protocol adds an additional approx. of 35% of data apart from final formatted data in RAM Module.

Results Discussion and Analysis

For the increase in the data sample size, functional blocks RX Function, FIFO and RAM Modules have been configured. The data stored in the RAM Module is obtained using system log and the checksum is obtained from it.

SignalTap II logic analyzer is used to obtain checksum for the configured system. The obtained checksum is compared with the checksum obtained from the log and found to be same. This confirms the complete data transfer for the configured Data Acquisition FPGA. (Figure 4). The system was tested by triggering scans at various sampling frequencies. The data being transferred are observed from the logs .

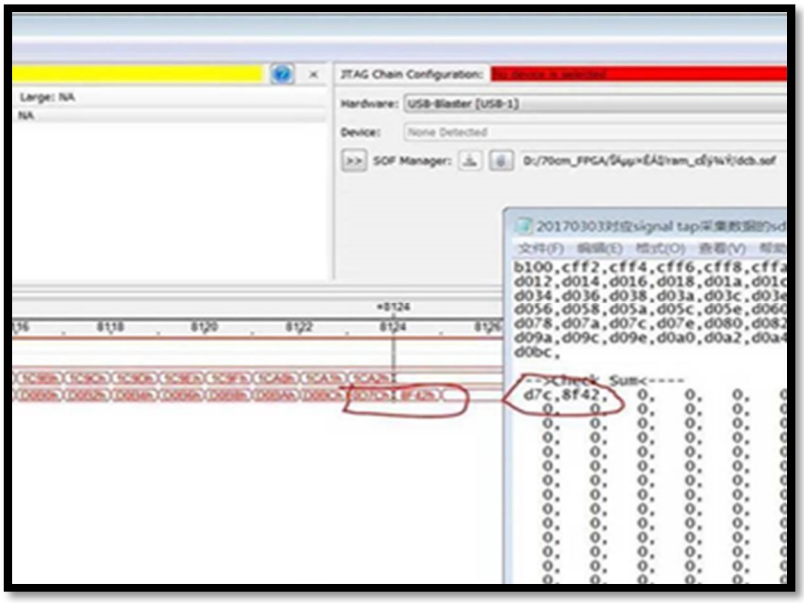

Figure 4 Checksum Check for RAM Module C

STUB:int CDpDevice:acknowledge(true) 546
scan seq 151000 transmitting 190061568 bits @ 984.00 Hz
collect_bytes: true

Figure 5: Data Rate Obtained for Sampling Frequency 984.0 for Existing Data Acquisition System

From the data rate results shown, the amount of data being processed per second can be viewed . For example, the data rate obtained for sampling frquency of 984 is approx. 190 Mbps. Now , adding the 35 % additional increase caused by FEC coding and CIMT protcol , the data rate is 257 Mbps.In the new Data Acquisition System with the increase in the data sample size, the data rate increased by 15 % from the base of 257 Mbps. (Figure 6 (a)).

STUB:int CDpDevice:acknowledge(true) 546
scan seq 3000 transmitting 220541952 bits @ 984.00 Hz
collect_bytes: true

Figure 6(a) Data Rate Obtained for Sampling Frequency 984.0 for Proposed Data Acquisition System

STUB:int CDpDevice:acknowledge(true) 546
scan seq 44000 transmitting 294055936 bits @ 1312.00 Hz
collect_bytes: true

Figure 6(b) Data Rate Obtained for Sampling Frequency 1230.0 for Proposed Data Acquisition System

STUB:int CDpDevice:acknowledge(true) 546
scan seq 43000 transmitting 275677440 bits @ 1230.00 Hz
collect_bytes: true

Figure 6(c) Data Rate Obtained for Sampling Frequency 1312.0 for Proposed Data Acquisition System

Then , data rates at various sampling frequencies like 1230, 1312, 1968 ,2460 and 2811 were observed. By increasing the sampling rate from 984 to 2460 , the data rate obtained was 551 Mbps. The obtained results for variuos sampling rates is shown in Figure 6(b),6(c),6(d),6(e).
With the obtained 551 Mbps, calculating the 35 % additional data added by the FEC Module and the CIMT transmission protocol, results in data rate of 748 Mbps. Further increase in the sampling rate of 2811.0 results in a data rate of 834 Mbps (634 Mbps +35% increase) which is beyond the hardware capacity.

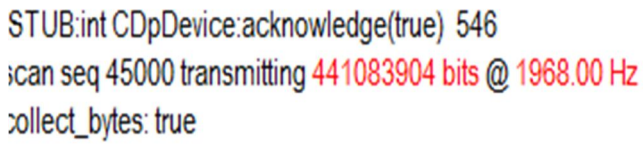

Figure 6(d) Data Rate Obtained for Sampling frequency 1968.0 for Proposed Data Acquisition System

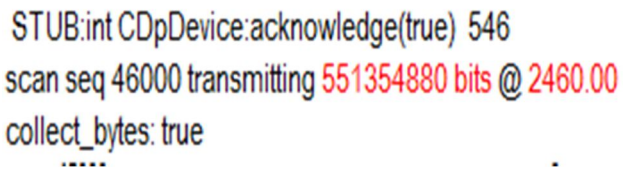

Figure 6(e) Data Rate Obtained for Sampling frequency 2460.0 for Proposed Data Acquisition System

By integrating the various factors such as increasing the data sample size and increasing the sampling frequency, the data rate of the system was increased by 191 % compared to the existing capacity. The maximum data rate was attained by increasing the sampling frequency from 984.0 to 2460.0.

Conclusion

In this paper, a high-speed Data Acquisition System for CT Scanners is presented. The existing Data Acquisition System was configured for increased data sample size. The proposed Data Acquisition System is capable of handling increased data rates and achieves maximum data rates that can be supported by present hardware. The proposed system has several advantages such as it could be extended for different gantry rotation times, for multi-slice detector etc.

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References

[1] Guzmain De Leon, J. A. Hernaindez Peralta, D. Rojas Montes De Oca and M. Cadena Mendez., “CT- Projections Hardware Raw Data Acquisition System for Image Reconstruction”, International Conference on Electrical and Electronics Engineering ,2007, ISBN: 1-4244-1166-1
[2] Anju P. Raju, Ambika Sekhar, “Implementation of High Speed Distributed Data Acquisition System”, International Journal of Advancements in Research & Technology, Volume 1, Issue 4, September-2012 1 ISSN 2278-7763
[3] Jan Dolinay, Petr Dostálek, Vladimír Vašek, , “Simple Data Acquisition Unit for School Laboratory Exercises”, *12th* International Carpathian Control Conference,2011, pp.85-88
[4] Abdelkader Bousselham, “FPGA Based Data Acquisition System and Digital Pulse Processing for PET and SPECT”, 2007, Stockholm: Fysikum , 76 p, ISBN: 91-7155-382-7
[5] Jonathan Alan Murray,Thomas Robert Murray, Paul Charles Schanen ,General Electric Company, “Scalable data acquisition system”,1998, Patent No :EP0994428 A3
[6] Tin-Su Pan, General Electric Company, “Methods and apparatus for efficient Data Acquisition in CT Scanners”, 2001, Patent No: US 6272201 B1
[7] Kalender W, Seissler W, Klotz E, Vock P, “Spiral volumetric CT with single-breath-hold technique, continuous transport and continuous scanner rotation”,1990, Radiology 176:181-183
[8] Hu H, “Multi-slice helical CT: Scan and Reconstruction”,1999, Med Phys 26:5-18

[9] Hu H, He HD, Foley WD, Fox SH, “Four multidetector row helical CT: Image quality and volume coverage speed”, 2000, Radiology 215: 55-62
[10] Thomas Flohr, Stefan Ulzheimer, “Multislice CT: Current Technology and Future Developments”, Multislice CT, Springer Berlin Heidelberg; p. 3–23
[11] CT literature, www.wiki.health.ge.com
[12] GE Healthcare India, www3.gehealthcare.in